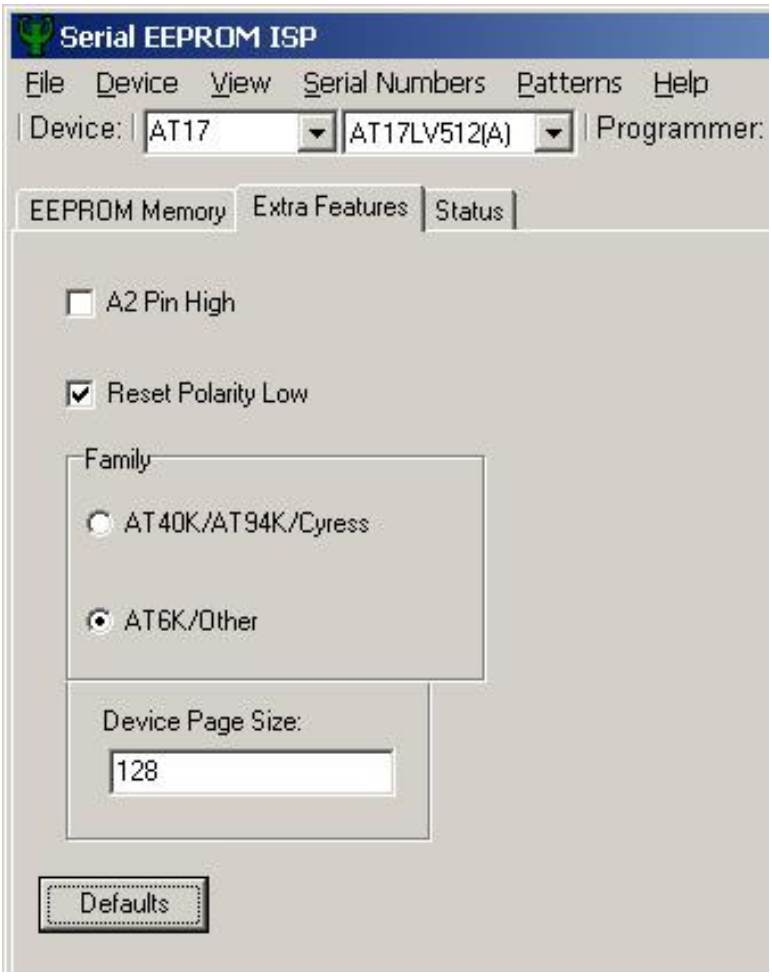
AT17LVxxx and AT17Fxxx User Guide

Select AT17 in Device drop Down and select your particular device in next drop down. A and non-A parts have slightly different pin-outs but are the same for ISP.

Extra Features tab



1) A2 pin setting (0 or 1) for cascaded devices, default low (0).

2) Reset Polarity (AT17LV512 and larger devices). Default is Reset Polarity Low. For High Reset Polarity, uncheck box then program the device. Program Reset polarity is part of device program operation. To verify it, choose **Device Menu -> Verify -> Reset Polarity.**

3) **Family**: Choose type of FPGA to be used with the AT17 chip. Default is AT6K/Other, which includes Xilinx chips. Xilinx parts are programmed LSBit first not MSB first like AT40K series. Xilinx MCS and HEX files are saved and loaded into the programmer buffer MSBit first but the AT17 device is programmed and read LSB first.

4) Device Page Size (only AT17LVxxx) is default programming page size and should not need changing.

5) AT17LV erased parts read all 0x00. AT17F parts read 0xFF like other EEPROMs.

6) Defaults Button will reload default values for the other options.

Device Menu

Erase is required for AT17Fxxx devices before they can be programmed but not for AT17LVxxx. Erase typically takes 33 seconds.

Device Menu -> Auto Program Options can be used to set what operations to carry out when Auto Program (F5 key) is selected.

AT17LVxxx devices have Reset Polarity, except ATLV256(A). Value is set on Extra Features tab and it is programmed with the rest of the program operation. To verify it, choose Device menu -> Verify -> Reset Polarity

AT17LV512A, AT17LV010A and AT17LV002A have option to enable or disable the Internal RC. Standard parts do not have this feature.

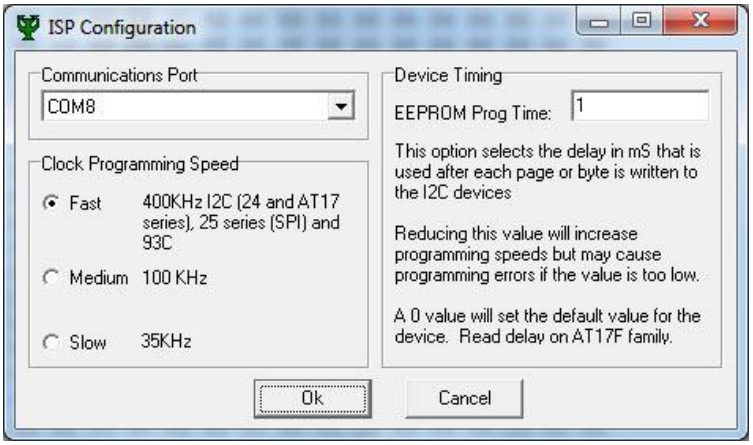
Device menu -> Program -> Internal RC Enabled - A parts only
Device menu -> Program -> Internal RC Disabled - A parts only

Options Button

Clicking the Options button brings up the Options Dialog. The available COM ports are displayed. On computers without serial ports these will be USB virtual serial ports and your programmer will be shown here *if it is plugged in!*

The other features are slightly different for AT17LVxxx and AT17Fxxx devices.

AT17LVxxx Settings

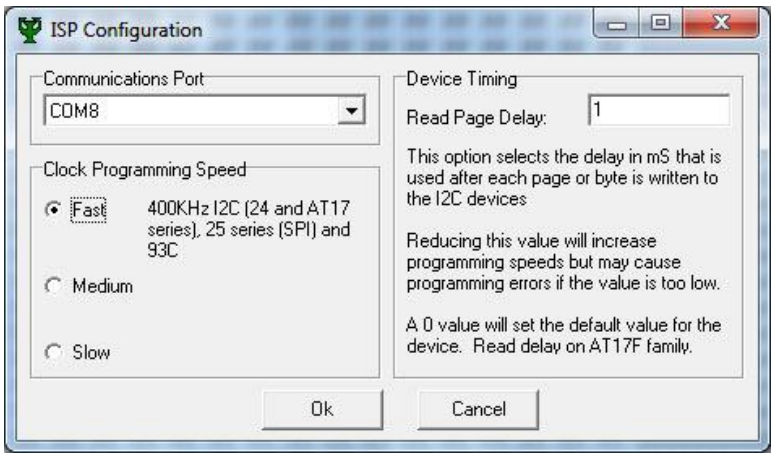


This is the same as other EEPROMs. You should not need to change these settings as AT17LVxxx devices have 400KHz I2C interface for programming. **The EEPROM Prog Time** is the delay between page writes and is set for default time needed.

If you get verify errors, you can try a slower speed or increase EEPROM Prog Time.

AT17Fxxx Settings

These chips have slightly different settings. The COM port setting is the same but the other two settings are slightly different.



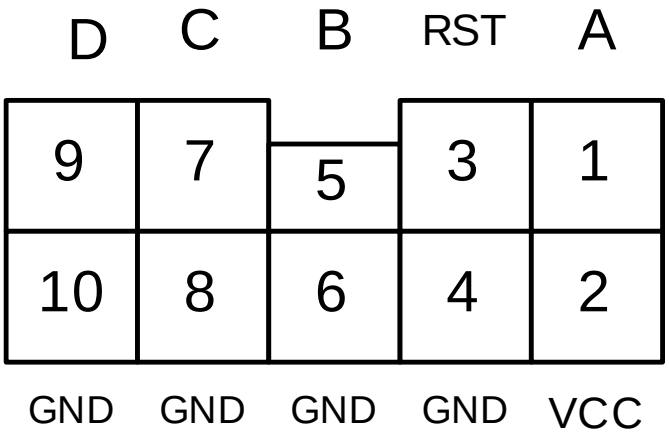
The Clock Programming Speed setting is 400KHz on Fast, but Medium and Slow settings are not a specific frequency, just a bit slower. Select these if you get verify errors.

The other setting is Read Page Delay. This is the delay between different read blocks. The device is read in 8KB blocks. If you get verify errors, you may need to increase this value. Reducing the value will reduce read time. The default is 100mS.

Connection Information

Data line must have 4K7 pull up, Clock can have 4K7 pull up

The end of the 10-way lead has this pin out



Where A,B,C,D and RST are defined for different device families

	24C (I2C)	25C (SPI)	93C (MicroWire)	AT17
A	N/C	SI	DI	SER_EN
B	N/C	CS	CS	N/C
C	SCL	SCK	CLK	SCLK
D	SDA	SO	DO	DATA
3	Micro RST	Micro RST	Micro RST	

At least one Ground and VCC must be connected to programmer.

Flying Lead Connector

The flying lead connector can be used to connect to other ISP connectors.

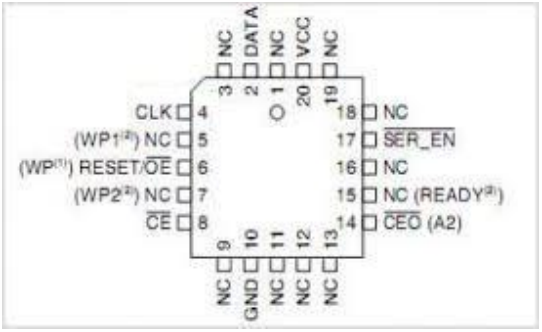
PIN	COLOUR	I2C	MICROWIRE	SPI	AT17
1	ORANGE		SI	DI	SER_EN
2	RED		CS	CS	
3	GREEN	VCC	VCC	VCC	VCC
4	BROWN	GND	GND	GND	GND
5	BLUE	SDA	DO	SO	DATA
6	YELLOW	SCL	CLK	SCK	SCLK

AT17 Devices

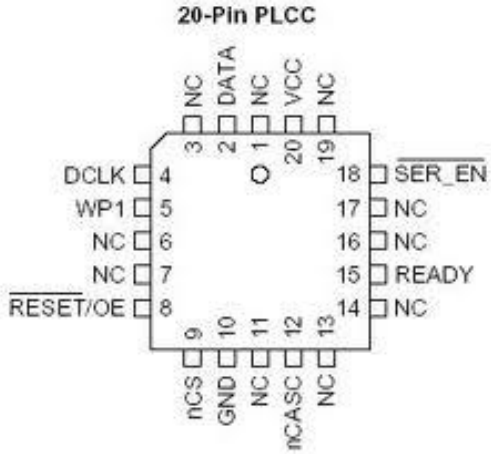
If SER_EN pin is grounded on target board, the orange SER_EN wire can be omitted.

AT17 chips need pull ups (4K7) on data line (blue wire) and sometimes on clock line (yellow).

AT17 standard pin layout

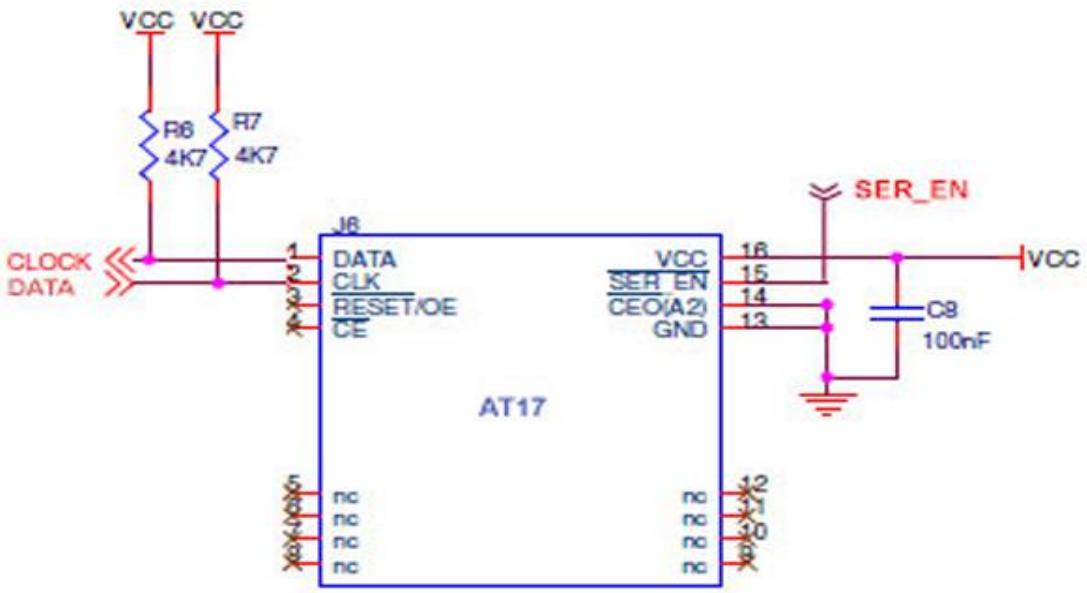


AT17 A parts pin out



Pull-up CEO/A2 pin for 0xAE I2C Address. Pull-down CEO/A2 pin for 0xA6 (4.7 k□) and match with A2 pin high or low in software. Different addresses allow two AT17 devices to be used in same circuit.

Typical AT17 ISP Circuit



Flying Lead Connections

CLOCK – YELLOW
DATA -- BLUE
SER_EN – ORANGE
VCC -- GREEN
GND -- BROWN

AT17 Connected to FPGA

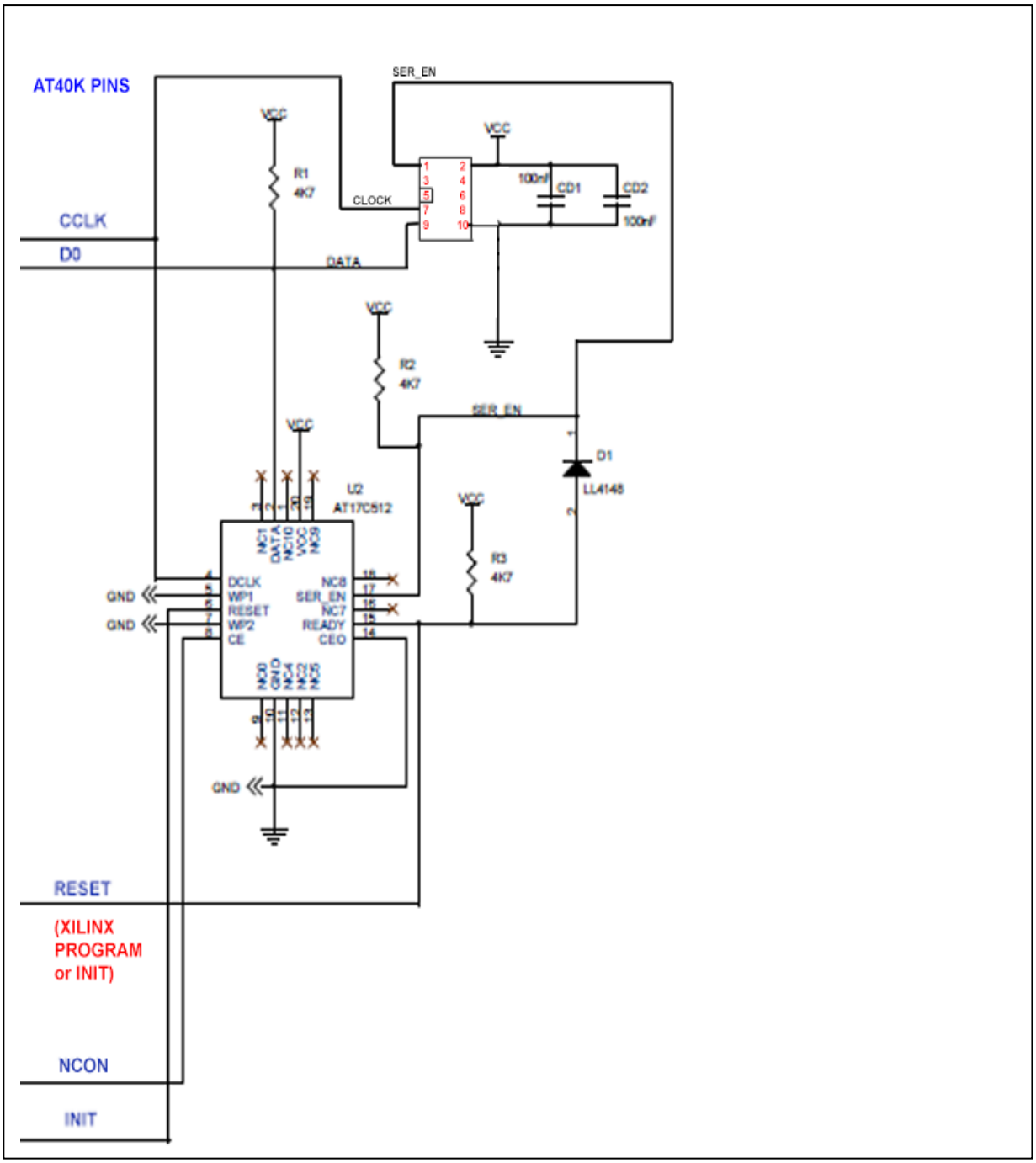
Although the programmer controls SER_EN, which puts AT17 configuration EEPROM into ISP mode, any connected FPGA will still interfere with the ISP operation unless control lines on the FPGA are connected to ISP circuit or grounded.

This circuit connects AT17 SER_EN, which is driven low by programmer, to FPGA control line to suspend its operation to allow ISP to work. The diode provides Open Drain output, which is recommended but not essential.

For AT40K family it connects SER_EN to RESET. For ZILINX FPGAS, connecting either PROGRAM or INIT pins instead will cause them to go low and hold the device in memory clearing phase. This allows AT17 to be programmed as programmer holds SER_EN low.

AT17 RESET and CE pins are connected as required for FPGA operation but do not affect programming..

Typical FPGA – AT17 ISP Circuit. (AT40K20 FPGA)



This circuit shows a 10-way ISP connector from programmer. For flying lead connections instead, pins on ISP header are:

Pin 1 is SER_EN = Orange
Pin 9 is Data = Blue
Pin 7 is Clock = Yellow
Pin 1 is VCC = Green
Pin 10 (or 4,6, 8) is GND = Brown

FPGA Clock and Data pins should be connected to AT17 and ISP header, with 4K7 pull-ups, optional on Clock line.

AT17 chip should be mounted as close as possible to FPGA.

Conclusion
Programmer puts AT17 SER_EN pin low to enable ISP. This circuit connects SER_EN to FPGA via optional diode to put FPGA in Reset or to suspend it, RESET on AT40K, PROGRAM or INIT pins on Xilinx devices.

Alternatively, you can manually ground INIT, RESET or PROGRAM during programming operations.